**Indira Gandhi Delhi Technical University For Women**
**(Established by Govt. of Delhi vide Act 09 of 2012)**
**Kashmere Gate, Delhi-110006**
**Department of Electronics & Communication Engineering**

F-AD-03

# TIME TABLE

**Odd Sem. August –Dec 2021/ B.Tech 1st Semester M Tech (VLSI)** **w.e.f: 9th Aug,2021**

| Time / Day | 9-10 AM | 10-11 AM | 11-12 AM | 12-1 PM | 1-2 PM | 2-3 PM | 3-4 PM | 4-5 PM |
|---|---|---|---|---|---|---|---|---|
| Mon | RM | | | | SDDIC | CMOS | AIC | HDL |
| Tue | RM | | | | | CMOS | AIC | |
| Wed | | | | | | CMOS | AIC | HDL |
| Thu | RM | | HDL Lab | | | SDDIC | AIC(T) | HDL |
| Fri | | | CMOS Lab | | | SDDIC | SDDIC Lab | |

| Sub. Code | Lab/ Course Name | Faculty Name | Lab Staff |
|---|---|---|---|
| MVD-101 | CMOS Analog Circuit Design (CMOS) (Th+Lab) | GF | |
| MVD-103 | Semiconductor Devices for DIC (SDDIC)(Th+Lab) | GF | |
| MVD-105 | Hardware Description Language (HDL) (Th+Lab) | Dr Shobha Sharma | |
| MVD-107 | Advanced IC Processing (AIC) | Prof Vandana Niranjan | |
| ROC-101 | Research Methodology (RM) | Dr Dinesh Ganotra | |

**Prof Nidhi Goel**
**(HOD, ECE)(Time Table In-charge, ECE Dept)**

**Ms Greeshma Arya**

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F-AD-03

# TIME TABLE

**Odd Sem. August –Dec 2021/ B.Tech 3rd Semester M Tech (VLSI)** **w.e.f: 9th Aug,2021**

| Time / Day | 9-10 AM | 10-11 AM | 11-12 AM | 12-1 PM | 1-2 PM | 2-3 PM | 3-4 PM | 4-5 PM |
|---|---|---|---|---|---|---|---|---|
| Mon | | | | ASIC | | | | VLSI Interconnect |
| Tue | | | | VLSIDVT | | | | |
| Wed | VLSI Interconnect | | ASIC | VLSIDVT | | | | |
| Thu | | | | ASIC | ASIC Lab | | | VLSI Interconnect |
| LPVD Lab | | | | VLSIDVT | VLSIDVT(T) | | | VLSI Interconnect (T) |

| Sub. Code | Lab/ Course Name | Faculty Name | Lab Staff |
|---|---|---|---|
| MVD-201 | ASIC and SOC Design (ASIC) (Th+Lab) | Prof Nidhi Goel | |
| MVD 213 | VLSI interconnect | Prof Jasdeep Kaur | |
| MVD 205 | VLSIDVT | Prof Vandana Niranjan | |

**Prof Nidhi Goel**
**(HOD, ECE)(Time Table In-charge, ECE Dept)**

**Ms Greeshma Arya**